Digital Array Radar Technology for Low Cost Radar

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Working Group for Multifunction Phased Array Radar Meeting
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Outline

• Introduction to Digital Array Technology
  • Moore’s Law, Cost, and Performance
  • Low-Cost RF Frontend Concept

• Army DAR Project
  • Digital Beamforming and Adaptability
  • GaN Antenna Panel Integration
  • Digital Backend Enhancements

• DARPA Efforts Related to Low-Cost Radar
Phase shifter/attenuator per element
- Enables fast beam switching
- Losses on both Tx. & Rx.
- Fixed, metal beamformer
- Single points of failure

Introduction: Digital Array Radar

Past: Passive Array

Analog Beamformer

HP Duplexer

LNA

Receiver and A/D

Tube Amp

Waveform Generator

Processor & Controller

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Present: Active Array (Digitized Subarray)
- LNA, HPA, phase shifter, attenuator, duplexer, T/R switches per element
- All RF parts handle less power
- Lower RF losses
- More waveform agility
- "Graceful degradation"
- Multiple beams possible w/adaptivity
- Mixing/digitization at subarrays

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- Transceiver, digitizer, and DDS for each element
- Multiple beams and adaptive beamforming limited by I/O and processing only, not RF hardware
- Ultimate in waveform agility
- High dynamic range potential
- Multiple concurrent functions


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Future/Now: Digital Array

Advanced Integration

Difficult to functionally “separate” the sections

Future Digital Arrays

- Lower cost
  - panelization of RF + digital
  - modular/open architecture
  - highly-integrated RF with direct-conversion/low IF
  - surface mount technology and plastic packaging

- Advanced functionality
  - digital at each element
  - distributed transceivers
  - self-monitoring of errors
  - multiple functions
  - dual polarization (MPAR)
  - More I/O and processing BW

Future challenge: Leverage increasing role of digitization to overcome limitations of lower-cost RF and transceiver functions
With standardized Intermediate Frequency’s, you can certainly envision a standardization of the entire IF/A to D/ Digital Beamformer Module.
Catching the World’s Cost Reduction

- FPGAs subject to the same implications of Moore’s Law as other digital circuits
- Performance and functionality improvements derived from increased transistor count
- Current FPGAs achieve needed functionality with costs reducing over time
  - Technology demonstrator at ~$15 per chip and falling
  - Processing technologies provide ASIC like performance at a reduced cost while allowing for FPGA prototyping ease
    - Xilinx EasyPath
    - Altera HardCopy


http://www.xilinx.com/partners/90nm/

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Software programmability – New beamforming and scan strategies. Dynamic beamforming capabilities.

Hardware programmability - monthly/yearly adaptability
Low Cost RF

What has changed in the RF world that makes low cost possible now:

1) RF has in some ways become a commodity, silicon dominates the RF landscape
2) Full wave electromagnetic analysis has became commonplace
3) Digital functions and capabilities increasingly important in the RF design space
4) III-V is starting to be dominated by wideband gap semiconductors

There is the potential for RF to be very cheap. For the first time, the RF circuit is not the domain of the specialist.
Low-Cost Array Concept

Traditional Hybrid Radar Module

Advanced Integration

Digital Backend

Traditional electronics

Massively integrated SiGe chip transceivers

High power GaN MMIC

Want low cost integration without sacrificing performance.

Key technologies are GaN, SiGe, and digital backend integrated using traditional electronics manufacturing techniques

Image from Eurofighter’s radar http://www.airpower.at/news06/0922_captor-e/index.html
**A Specific Example: Army DAR Project**

Vision for S-band digital subarray

Initial subarray demonstrator

- Antenna Array and HPA/LNA Panel
- Transceiver Boards
- Control Board
- Quadrant Boards

Control

- PC
- RS-232
- JTAG
- Spartan 3AN FPGA
- 32 Mb SRAM
- Clock Dist.

Quadran

- Spartan 3A FPGA
- 2x DAC
- 4x ADC
- Xcvr. Header
- 32 Mb SRAM

Transceiver

- 2x2 MIMO Xcvr.
- Head
- 2x2 MIMO Xcvr.

RF

- Sw.
- GaN
- Sw.
- GaN
- Sw.
- GaN

Five graduate students, two undergraduates, and two faculty

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Initial DAR Demonstrator

16-Element Backend Stats:

- Frequency: 3.1-3.5 GHz
- Inst. BW: 14 MHz direct conversion
- Antenna Board: Rogers 4350b & Rohacell
- Antenna Type: Stacked patch (apt. fed)
- Backend PCBs: FR-4
- A/D resolution: 12 Bits
- Sample rate: 24 Msps (I/Q)
- Control Intfc.: MATLAB (RS-232)
- Data Intfc: Gigabit Ethernet
- Real-time beams: 1 (sum/difference)
- Element-level RAM: 32 Mb

GaN Panel Stats:

- GaN HPA power: 25 W @ 28V per element
- GaN HPA PAE: >60%
Initial DAR Demonstrator

Integrated Ant./RF Panel
Initial DAR Demonstrator

Two Channel SiGe Transceivers

Integrated Ant./RF Panel

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Initial DAR Demonstrator

- Data Conversion/Processing
- Two Channel SiGe Transceivers
- Integrated Ant./RF Panel
Initial DAR Demonstrator

- Digital Backend/PC Interface
- Data Conversion/Processing
- Two Channel SiGe Transceivers
- Integrated Ant./RF Panel
Initial DAR Demonstrator

- **System Controls**: Software Loader, Calibration Loader, Register Loader, System Loader, OB bin, CB bin, ADC, Ref. Serial, RAM Chk.
- **Transmitter Controls**: Transmitter Weighting, Transmitter Calibration, Transmitter SM Controls, BB Filter BW (MHz), Global DAC Disable, Pulse On.
- **SMI Board Controls**: SMI Controls, PA A En., PA Step A, TR A, Rx En., PA B En., PA Step B, TR B, Tx En., Rx OR, Rx R, Sys. RX A, TX A, RX B, TX B, Gen. B.
- **Data Conversion/Processing**: Digital Backend/PC Interface.
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DAR Digital Beamforming

- Verified digital beamforming on Tx. & Rx.
- Measured patterns at Lockheed Martin

16 elements demonstrated with transmit and receive. Independent digitization of each transmit and receive channel
Army DAR Project Digital Backend

• Important features
  • Digital at every element
  • Standard PCB processing
  • Hierarchical digital beamformer
  • Distributed direct-conversion transceivers

• Simple example: Bi-static tracking

\[ V_T[n] = \sum_{m=1}^{8} \frac{R_m'}{R_m} V_m[n] + S[n] \]

Coupling & clutter suppression with element-level data

Error in Tracking Angle and Target to Clutter Ratio

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Automated Adaptability

- Principle of operation:
  - Use receivers as built-in vector signal analyzers
  - Monitor transmit-receive coupling pair signals

- Applications:
  - Array self-calibration and calibration monitoring
  - Built-in/automatic I/Q imbalance correction

- Example:
  - Denote initial (complex) coupling to n<sup>th</sup> receiver from the m<sup>th</sup> transmitter as $C_{mn}$
  - After array has been fielded, make the same recordings ($C_{mn}'$), forming the matrix $K$:
    \[ C_{mn}' \approx T_m R_n C_{mn} \quad K_{nn} = \frac{C_{mn}'}{C_{mn}} \approx T_m R_n \]
    \[ T_m = \text{error from digital signal to } V_m \text{ on Tx.} \]
    \[ R_n = \text{error from } V_n \text{ to digital signal on Rx.} \]
  - Use this matrix to estimate errors in the array (see example $\rightarrow$)

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Automated Adaptability

\[ \mathbf{K} \approx \begin{bmatrix} T_1 R_1 & T_1 R_2 & T_1 R_3 & T_1 R_4 & T_1 R_5 & T_1 R_6 & T_1 R_7 & T_1 R_8 \\ T_2 R_1 & T_2 R_2 & T_2 R_3 & T_2 R_4 & T_2 R_5 & T_2 R_6 & T_2 R_7 & T_2 R_8 \\ T_3 R_1 & T_3 R_2 & T_3 R_3 & T_3 R_4 & T_3 R_5 & T_3 R_6 & T_3 R_7 & T_3 R_8 \\ T_4 R_1 & T_4 R_2 & T_4 R_3 & T_4 R_4 & T_4 R_5 & T_4 R_6 & T_4 R_7 & T_4 R_8 \end{bmatrix} \]
Automated Adaptability

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Initial

\[ T = 36 \text{C} \]
Automated Adaptability

$K \approx \begin{bmatrix} T_1R_1 & T_1R_2 & T_1R_3 & T_1R_4 & T_1R_5 & T_1R_6 & T_1R_7 & T_1R_8 \\ T_2R_1 & T_2R_2 & T_2R_3 & T_2R_4 & T_2R_5 & T_2R_6 & T_2R_7 & T_2R_8 \\ T_3R_1 & T_3R_2 & T_3R_3 & T_3R_4 & T_3R_5 & T_3R_6 & T_3R_7 & T_3R_8 \\ T_4R_1 & T_4R_2 & T_4R_3 & T_4R_4 & T_4R_5 & T_4R_6 & T_4R_7 & T_4R_8 \end{bmatrix}$

Initial

$T = 36C$

$T = 39C$
Automated Adaptability

\[ K \approx \begin{bmatrix} T_1 R_1 & T_1 R_2 & T_1 R_3 & T_1 R_4 & T_1 R_5 & T_1 R_6 & T_1 R_7 & T_1 R_8 \\ T_2 R_1 & T_2 R_2 & T_2 R_3 & T_2 R_4 & T_2 R_5 & T_2 R_6 & T_2 R_7 & T_2 R_8 \\ T_3 R_1 & T_3 R_2 & T_3 R_3 & T_3 R_4 & T_3 R_5 & T_3 R_6 & T_3 R_7 & T_3 R_8 \\ T_4 R_1 & T_4 R_2 & T_4 R_3 & T_4 R_4 & T_4 R_5 & T_4 R_6 & T_4 R_7 & T_4 R_8 \end{bmatrix} \]

Initial

\[ T = 36 \text{C} \quad T = 39 \text{C} \quad T = 45 \text{C} \]
Automated Adaptability

$K \approx \begin{bmatrix} T_1 R_1 & T_1 R_2 & T_1 R_3 & T_1 R_4 & T_1 R_5 & T_1 R_6 & T_1 R_7 & T_1 R_8 \\ T_2 R_1 & T_2 R_2 & T_2 R_3 & T_2 R_4 & T_2 R_5 & T_2 R_6 & T_2 R_7 & T_2 R_8 \\ T_3 R_1 & T_3 R_2 & T_3 R_3 & T_3 R_4 & T_3 R_5 & T_3 R_6 & T_3 R_7 & T_3 R_8 \\ T_4 R_1 & T_4 R_2 & T_4 R_3 & T_4 R_4 & T_4 R_5 & T_4 R_6 & T_4 R_7 & T_4 R_8 \end{bmatrix}$

Initial

$T = 36C$

$T = 50C$

Final
**Automated Adaptability**

Radar can self-correct for environmental stresses:

- **Tx**: +/- 5 deg. & 0.13 dB
- **Rx**: +/- 2.0 deg. & 0.2 dB

### Initial Temperatures

- **T = 36°C**
- **T = 39°C**
- **T = 45°C**
- **T = 50°C**

### Radar System

The radar system is represented by a matrix 

\[ K \approx \begin{bmatrix} T_1R_1 & T_1R_2 & T_1R_3 & T_1R_4 & T_1R_5 & T_1R_6 & T_1R_7 & T_1R_8 \\ T_2R_1 & T_2R_2 & T_2R_3 & T_2R_4 & T_2R_5 & T_2R_6 & T_2R_7 & T_2R_8 \\ T_3R_1 & T_3R_2 & T_3R_3 & T_3R_4 & T_3R_5 & T_3R_6 & T_3R_7 & T_3R_8 \\ T_4R_1 & T_4R_2 & T_4R_3 & T_4R_4 & T_4R_5 & T_4R_6 & T_4R_7 & T_4R_8 \end{bmatrix} \]
Automated Adaptability

Matrix Rotation to compensate for phase and amplitude

Beamforming (Sum and Difference)

T = 50C
I/Q Imbalance Self-Correction

- Automated I/Q compensation
- Demonstrates $\sim 10\log(N)$ improvement at beam peak
- Enables use of low-cost components
Matrix Rotation to compensate for phase and amplitude

DC subtraction
I/Q imbalance

Beamforming (Sum and Difference)

\[
\begin{bmatrix}
I[n] \\
Q[n]
\end{bmatrix} = A \begin{bmatrix}
I[n] \\
Q[n]
\end{bmatrix} - \begin{bmatrix}
I_{DC} \\
Q_{DC}
\end{bmatrix} + B \begin{bmatrix}
I[n-1] \\
Q[n-1]
\end{bmatrix} - \begin{bmatrix}
I_{DC} \\
Q_{DC}
\end{bmatrix}
\]
Massive integration has taken place and promises to further consume components

Currently available from Analog Devices

Potential Re-Configurable HDB Capabilities

- Dynamic subarray allocation & array partitioning of T/R

Examples:
- Simultaneous T/R with coupling cancellation

Intermediate beamformer

Final beam-former + RSP

Arbitrary, dynamic, subarray allocation to minimize and randomize grating lobes over time

Examples:
- Normal Radar
- Guard Cells
- Rx across full spectrum

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Current Related DARPA Programs
What else may impact cost further?

Compound Semiconductor Materials on Silicon (COSMOS)

**Program Objective:** Heterogeneous integration all the way to the transistor scale
- Enable materials selection within circuits — without loss of transistor performance
- Exploit existing SOA CMOS infrastructure & integration levels — without process modification

**DoD Benefits**
- Achieve higher functional density: dense integration of analog, mixed-signal, & digital electronics
- Enable circuits with lower dissipated power & far higher I/O throughput

Today

Flip-chip
Reflow solder bumps

*Chip size ~5 mm
*200 μm pitch

COSMOS Vision

Heterogeneous integration exists only on a very coarse scale – and not in the signal path

Allow the circuit designer to select the optimal transistor technology everywhere in the circuit
Microscale Power Conversion

Today: Fixed power supply voltage

Future: Dynamic microscale power conversion

Technical Area I: Power switch device and process integration

**Goals**

- Operating Voltage: > 50 V
- Threshold Voltage: > 1 V
- Power Handling: 10 W
- Off-State Gate Leakage Current: < 1.0 μA/mm
- Output Voltage Slew Rate: > 500 V/ns

Technical Area II: RF transmitter and supply modulation co-design & prototyping

**Goals**

- Frequency of RF Power Amplification: > 10 GHz
- RF Output Power: > 5 W
- Average PAE: > 75%
- PA RF envelope bandwidth: > 500 MHz
Conclusions

• I am optimistic that a path to low cost phased array radar will be found

• Digital radars, over time, can lead to lower cost by catching the cost reductions inevitable in the digital domain.

• I believe that we need a larger demonstrator that has cost as the primary goal to see what the performance/cost tradeoff actually would be.

But it is just a start. We need to show standardization/generalized design practices can impact the array world.